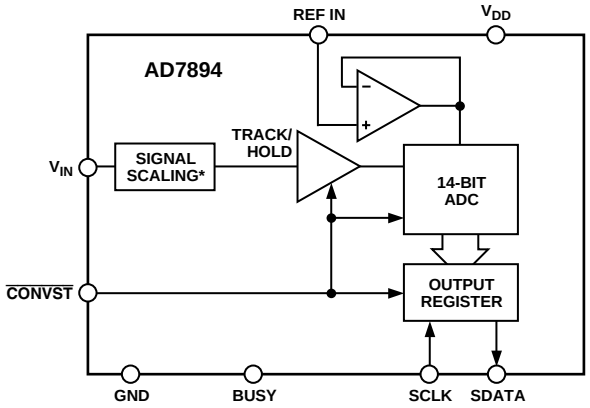
5 V, 14-Bit Serial, 5 μs ADC in SO-8 Package

AD7894

FEATURES

Fast 14-Bit ADC with 5 μs Conversion Time
8-Lead SOIC Package
Single 5 V Supply Operation
High Speed, Easy-to-Use, Serial Interface
On-Chip Track/Hold Amplifier
Selection of Input Ranges
±10 V for AD7894-10
±2.5 V for AD7894-3
0 V to +2.5 V for AD7894-2
High Input Impedance
Low Power: 20 mW Typ
Pin Compatible Upgrade of 12-Bit AD7895

FUNCTIONAL BLOCK DIAGRAM



*AD7894-10, AD7894-3

GENERAL DESCRIPTION

The AD7894 is a fast, 14-bit ADC that operates from a single +5 V supply and is housed in a small 8-lead SOIC. The part contains a 5 μs successive approximation A/D converter, an on-chip track/hold amplifier, an on-chip clock and a high speed serial interface.

Output data from the AD7894 is provided via a high speed, serial interface port. This two-wire serial interface has a serial clock input and a serial data output with the external serial clock accessing the serial data from the part.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7894 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part accepts an analog input range of ±10 V (AD7894-10), ±2.5 V (AD7894-3), 0 V to +2.5 V (AD7894-2), and operates from a single +5 V supply consuming only 20 mW typical.

The AD7894 features a high sampling rate mode and, for low power applications, a proprietary automatic power-down mode where the part automatically goes into power-down once conversion is complete and "wakes up" before the next conversion cycle.

The part is available in a small outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Fast, 14-Bit ADC in 8-Lead Package
   The AD7894 contains a 5 μs ADC, a track/hold amplifier, control logic and a high speed serial interface, all in an 8-lead package. This offers considerable space saving over alternative solutions.
2. Low Power, Single Supply Operation
   The AD7894 operates from a single +5 V supply and consumes only 20 mW. The automatic power-down mode, where the part goes into power-down once conversion is complete and "wakes up" before the next conversion cycle, makes the AD7894 ideal for battery powered or portable applications.
3. High Speed Serial Interface
   The part provides high speed serial data and serial clock lines allowing for an easy, two-wire serial interface arrangement.

REV. 0

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AD7894–SPECIFICATIONS (V_{DD} = +5 V ± 5%, GND = 0 V, REF IN = +2.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal to (Noise + Distortion) Ratio[3]				
@ +25°C	78	78	dB min	f_{IN} = 70 kHz Sine Wave, f_{SAMPLE} = 160 kHz
T_{MIN} to T_{MAX}	77	77	dB min	See Figure 14
Total Harmonic Distortion (THD)[3]	–86	–86	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 160 kHz, Typically –87 dB. See Figure 15
Peak Harmonic or Spurious Noise[3]	–92	–92	dB typ	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 160 kHz
Intermodulation Distortion (IMD)[3]				fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 160 kHz
2nd Order Terms	–92	–92	dB typ	
3rd Order Terms	–92	–92	dB typ	
DC ACCURACY				
Resolution	14	14	Bits	
Minimum Resolution for Which				
No Missing Codes Are Guaranteed	14	14	Bits	
Relative Accuracy[3]	±2	±1.5	LSB max	
Differential Nonlinearity[3]	–1 to +1.5	–1 to +1.5	LSB max	
AD7894-2				
Positive Gain Error[3]	±12	±10	LSB max	
Unipolar Offset Error	±8	±6	LSB max	
AD7894-10, AD7894-3 Only				
Positive Gain Error[3]	±8	±6	LSB max	
Negative Gain Error[3]	±8	±6	LSB max	
Bipolar Zero Error	±10	±8	LSB max	
ANALOG INPUT				
AD7894-10				
Input Voltage Range	±10	±10	V	
Input Current	2	2	mA max	See Analog Input Section
AD7894-3				
Input Voltage Range	±2.5	±2.5	V	
Input Current	1.5	1.5	mA max	See Analog Input Section
AD7894-2				
Input Voltage Range	0 to +2.5	0 to +2.5	V	
Input Current	500	500	nA max	
REFERENCE INPUT				
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	1	1	µA max	
Input Capacitance[4]	10	10	pF max	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
Output Coding				
AD7894-10, AD7894-3	Twos Complement			
AD7894-2	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time				
Mode 1 Operation	5	5	µs max	
Mode 2 Operation[5]	10	10	µs max	
Track/Hold Acquisition Time[3]	0.35	0.35	µs max	
SAMPLE AND HOLD				
–3 dB Small Signal Bandwidth	7.5	7.5	MHz typ	
Aperture Jitter	50	50	ps typ	

Parameter	A Versions[1]	B Versions[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}	5.5	5.5	mA max	Digital Inputs @ V_{DD}, V_{DD} = 5 V ± 5%
Power Dissipation	27.5	27.5	mW max	Typically 20 mW
Power-Down Mode				
I_{DD} @ T_{MIN} to T_{MAX}	20	20	µA max	Digital Inputs @ GND, V_{DD} = 5 V ± 5%
Power Dissipation T_{MIN} to T_{MAX}	100	100	µW max	Typ 15 µW

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C.
[2]Applies to Mode 1 operation. See Operating Modes section.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]This 10 µs includes the "wake-up" time from standby. This "wake-up" time is timed from the rising edge of $\overline{\text{CONVST}}$, whereas conversion is timed from the falling edge of $\overline{\text{CONVST}}$, for narrow $\overline{\text{CONVST}}$ pulsewidth the conversion time is effectively the "wake-up" time plus conversion time, hence 10 µs. This can be seen from Figure 3. Note that if the $\overline{\text{CONVST}}$ pulsewidth is greater than 5 µs, the effective conversion time will increase beyond 10 µs.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, GND = 0 V, REF IN = +2.5 V)

Parameter	A, B Versions	Units	Test Conditions/Comments
t_1	40	ns min	$\overline{\text{CONVST}}$ Pulsewidth
t_2	31.25[2]	ns min	SCLK High Pulsewidth
t_3	31.25[2]	ns min	SCLK Low Pulsewidth
t_4	60[3]	ns max	Data Access Time after Falling Edge of SCLK V_{DD} = 5 V ± 5%
t_5	10	ns min	Data Hold Time after Falling Edge of SCLK
t_6	20[4]	ns max	Bus Relinquish Time after Falling Edge of SCLK

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
[2]The SCLK maximum frequency is 16 MHz. Care must be taken when interfacing to account for the data access time, t_4, and the setup time required for the user's processor. These two times will determine the maximum SCLK frequency with which the user's system can operate. See Serial Interface section for more information.
[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.0 V.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_6, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

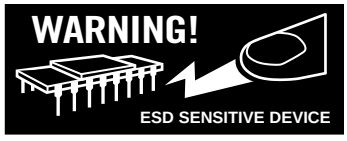
(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Analog Input Voltage to GND
AD7894-10 . . . . . ±17 V
AD7894-3 . . . . . ±7 V
AD7894-2 . . . . . –5 V to +10 V
Reference Input Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 170°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7894 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	INL	Input Range	SNR	Package Description	Package Option
AD7894AR-10	–40°C to +85°C	±2 LSB	±10 V	77 dB	8-Lead Narrow Body SOIC	SO-8
AD7894BR-10	–40°C to +85°C	±1.5 LSB	±10 V	77 dB	8-Lead Narrow Body SOIC	SO-8
AD7894AR-3	–40°C to +85°C	±2 LSB	±2.5 V	77 dB	8-Lead Narrow Body SOIC	SO-8
AD7894BR-3	–40°C to +85°C	±1.5 LSB	±2.5 V	77 dB	8-Lead Narrow Body SOIC	SO-8
AD7894AR-2	–40°C to +85°C	±2 LSB	0 V to +2.5 V	77 dB	8-Lead Narrow Body SOIC	SO-8

PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Mnemonic	Description
1	REF IN	Voltage Reference Input. An external reference source should be connected to this pin to provide the reference voltage for the AD7894's conversion process. The REF IN input is buffered on-chip. The nominal reference voltage for correct operation of the AD7894 is +2.5 V.
2	V_{IN}	Analog Input Channel. The analog input range is ±10 V (AD7894-10), ±2.5 V (AD7894-3) and 0 V to +2.5 V (AD7894-2).
3	GND	Analog Ground. Ground reference for track/hold, comparator, digital circuitry and DAC.
4	SCLK	Serial Clock Input. An external serial clock is applied to this input to obtain serial data from the AD7894. A new serial data bit is clocked out on the falling edge of this serial clock. Data is guaranteed valid for 10 ns after this falling edge so data can be accepted on the falling edge when a fast serial clock is used. The serial clock input should be taken low at the end of the serial data transmission.
5	SDATA	Serial Data Output. Serial data from the AD7894 is provided at this output. The serial data is clocked out by the falling edge of SCLK, but the data can also be read on the falling edge of SCLK. This is possible because data bit N is valid for a specified time after the falling edge of SCLK (data hold time) (see Figure 5). Sixteen bits of serial data are provided as two leading zeroes followed by the 14 bits of conversion data. On the 16th falling edge of SCLK, the SDATA line is held for the data hold time and then disabled (three-stated). Output data coding is twos complement for the AD7894-10 and AD7894-3, and straight binary for the AD7894-2.
6	BUSY	The BUSY pin is used to indicate when the part is doing a conversion. The BUSY pin will go high on the falling edge of $\overline{\text{CONVST}}$ and will return low when the conversion is complete.
7	$\overline{\text{CONVST}}$	Conversion Start. Edge-triggered logic input. On the falling edge of this input, the track/hold goes into its hold mode and conversion is initiated. If $\overline{\text{CONVST}}$ is low at the end of conversion, the part goes into power-down mode. In this case, the rising edge of $\overline{\text{CONVST}}$ will cause the part to begin waking up.
8	V_{DD}	Positive supply voltage, +5 V ± 5%.

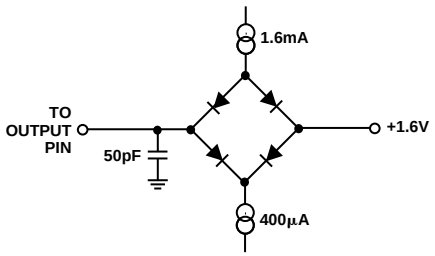
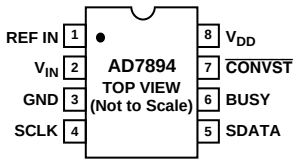


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PIN CONFIGURATION
SOIC (SO-8)



TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02\ N + 1.76)\ dB$$

Thus for a 14-bit converter, this is 86.04 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7894, it is defined as:

$$THD\,(dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. The value of this specification is normally determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither *m* nor *n* is equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb).

The AD7894 is tested using two input frequencies. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Gain Error (AD7894-10)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (4 × VREF – 1 LSB) after the Bipolar Zero Error has been adjusted out.

Positive Gain Error (AD7894-3)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (VREF – 1 LSB) after the Bipolar Zero Error has been adjusted out.

Positive Gain Error (AD7894-2)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal (VREF – 1 LSB) after the Unipolar Offset Error has been adjusted out.

Bipolar Zero Error (AD7894-10, AD7894-3)

This is the deviation of the midscale transition (all 0s to all 1s) from the ideal 0 V (GND).

Unipolar Offset Error (AD7894-2)

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal 1 LSB.

Negative Gain Error (AD7894-10)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (–4 × VREF + 1 LSB) after Bipolar Zero Error has been adjusted out.

Negative Gain Error (AD7894-3)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (– VREF + 1 LSB) after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the V_{IN} input of the AD7894. This means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CONVERTER DETAILS

The AD7894 is a fast, 14-bit single supply A/D converter. It provides the user with signal scaling, track/hold, A/D converter and serial interface logic functions on a single chip. The A/D converter section of the AD7894 consists of a conventional successive-approximation converter based around an R-2R ladder structure. The signal scaling on the AD7894-10 and AD7894-3 allows the part to handle ±10 V and ±2.5 V input signals respectively while operating from a single +5 V supply. The AD7894-2 accepts an analog input range of 0 V to +2.5 V. The part requires an external +2.5 V reference. The reference input to the part is buffered on-chip. The AD7894 has two operating modes, the high sampling mode and the "auto-sleep" mode where the part automatically goes into sleep after the end of conversion. These modes are discussed in more detail in the Timing and Control Section.

A major advantage of the AD7894 is that it provides all of the above functions in an 8-lead SOIC package. This offers the user considerable space saving advantages over alternative solutions. The AD7894 typically consumes only 20 mW, making it ideal for battery powered applications.

Conversion is initiated on the AD7894 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the on-chip track/hold goes from track-to-hold mode and the conversion sequence is started. The conversion clock for the part is generated internally using a laser-trimmed clock oscillator circuit. Conversion time for the AD7894 is 5 µs in the high sampling mode (10 µs for the auto sleep mode), and the track/hold acquisition time is 0.35 µs. To obtain optimum performance from the part, the read operation should not occur during the conversion or during 250 ns prior to the next conversion. This allows the part to operate at throughput rates up to 160 kHz and achieve data sheet specifications.

CIRCUIT DESCRIPTION

Analog Input Section

The AD7894 is offered as three part types, the AD7894-10, which handles a ±10 V input voltage range, the AD7894-3, which handles input voltage range ±2.5 V and the AD7894-2, which handles a 0 V to +2.5 V input voltage range.

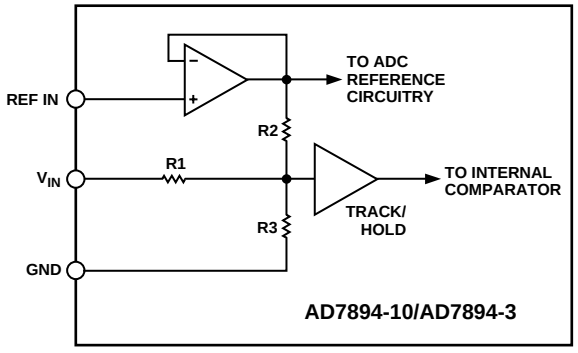


Figure 2. AD7894-10/AD7894-3 Analog Input Structure

Figure 2 shows the analog input section for the AD7894-10 and AD7894-3. The analog input range of the AD7894-10 is ±10 V and the analog input range for the AD7894-3 is ±2.5 V. This input is benign, with no dynamic charging currents as the resistor stage is followed by a high input impedance stage of the track/hold amplifier. For the AD7894-10, R1 = 8 kΩ, R2 = 2 kΩ and R3 = 2 kΩ. For the AD7894-3, R1 = R2 = 2 kΩ and R3 is open circuit. The current flowing in the analog input is directly related to the analog input voltage. The maximum input current flows when the analog input is at negative full scale.

For the AD7894-10 and AD7894-3, the designed code transitions occur on successive integer LSB values (i.e., 1 LSB, 2 LSBs, 3 LSBs . . .). Output coding is twos complement binary with 1 LSB = FS/16384. The ideal input/output transfer function for the AD7894-10 and AD7894-3 is shown in Table I.

Table I. Ideal Input/Output Code Table for the AD7894-10/ AD7894-3

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 1 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 2 LSBs	011 . . . 101 to 011 . . . 110
+FSR/2 – 3 LSBs	011 . . . 100 to 011 . . . 101
GND + 1 LSB	000 . . . 000 to 000 . . . 001
GND	111 . . . 111 to 000 . . . 000
GND – 1 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 3 LSBs	100 . . . 010 to 100 . . . 011
–FSR/2 + 2 LSBs	100 . . . 001 to 100 . . . 010
–FSR/2 + 1 LSB	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range = 20 V (AD7894-10) and = 5 V (AD7894-3) with REF IN = +2.5 V.
[2]1 LSB = FSR/16384 = 1.22 mV (AD7894-10) and 0.3 mV (AD7894-3) with REF IN = +2.5 V.

The analog input section for the AD7894-2 contains no biasing resistors and the V_{IN} pin drives the input directly to the track/hold amplifier. The analog input range is 0 V to +2.5 V into a high impedance stage with an input current of less than 500 nA. This input is benign, with no dynamic charging currents. Once again, the designed code transitions occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FS/16384 = 2.5 V/16384 = 0.15 mV. Table II shows the ideal input/output transfer function for the AD7894-2.

Table II. Ideal Input/Output Code Table for AD7894-2

Analog Input[1]	Digital Output Code Transition
+FSR – 1 LSB[2]	111 . . . 110 to 111 . . . 111
+FSR – 2 LSB	111 . . . 101 to 111 . . . 110
+FSR – 3 LSB	111 . . . 100 to 111 . . . 101
GND + 3 LSB	000 . . . 010 to 000 . . . 011
GND + 2 LSB	000 . . . 001 to 000 . . . 010
GND + 1 LSB	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 2.5 V for AD7894-2 with VREF = +2.5 V.
[2]1 LSB = FSR/16384 and is 0.15 mV for AD7894-2 with VREF = +2.5 V.

Track/Hold Section

The track/hold amplifier on the analog input of the AD7894 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 14-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC, even when the ADC is operated at its maximum throughput rate of 160 kHz (i.e., the track/hold can handle input frequencies in excess of 100 kHz).

The track/hold amplifier acquires an input signal to 14-bit accuracy in less than 0.35 µs. The operation of the track/hold is essentially transparent to the user. With the high sampling operating mode the track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion (i.e., the falling edge of $\overline{\text{CONVST}}$). The aperture time for the track/hold (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion (on the falling edge of BUSY) the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point. For the auto shutdown mode, the rising edge of $\overline{\text{CONVST}}$ wakes up the part and the track and hold amplifier goes from its tracking mode to its hold mode 5 µs after the rising edge of $\overline{\text{CONVST}}$ (provided that the $\overline{\text{CONVST}}$ high time is less than 5 µs). Once again the part returns to its tracking mode at the end of conversion when the BUSY signal goes low.

Reference Input

The reference input to the AD7894 is buffered on-chip with a maximum reference input current of 1 µA. The part is specified with a +2.5 V reference input voltage. Errors in the reference source will result in gain errors in the AD7894's transfer function and will add to the specified full-scale errors on the part. Suitable reference sources for the AD7894 include the AD780 and AD680 precision +2.5 V references.

Timing and Control Section

Figure 3 shows the timing and control sequence required to obtain optimum performance from the AD7894. In the sequence shown, conversion is initiated on the falling edge of $\overline{\text{CONVST}}$ and new data from this conversion is available in the output register of the AD7894 5 µs later. Once the read operation has taken place, a further 250 ns should be allowed before the next falling edge of $\overline{\text{CONVST}}$ to optimize the settling of the track/hold amplifier before the next conversion is initiated. With the serial clock frequency at its maximum of 16 MHz, the achievable throughput rate for the part is 5 µs (conversion time) plus 1.0 µs (read time) plus 250 ns (quiet time). This results in a minimum throughput time of 6.25 µs (equivalent to a throughput rate of 160 kHz). A serial clock of less than 16 MHz can be used, but this will in turn mean that the throughput time will increase.

The read operation consists of 16 serial clock pulses to the output shift register of the AD7894. After 16 serial clock pulses the shift register is reset and the SDATA line is three-stated. If there are more serial clock pulses after the 16th clock, the shift register will be moved on past its reset state. However, the shift register will be reset again on the falling edge of the $\overline{\text{CONVST}}$ signal to ensure that the part returns to a known state every conversion cycle. As a result, a read operation from the output register should not straddle across the falling edge of $\overline{\text{CONVST}}$ as the output shift register will be reset in the middle of the read operation and the data read back into the microprocessor will appear invalid.

OPERATING MODES

Mode 1 Operation (High Sampling Performance)

The timing diagram in Figure 3 is for optimum performance in operating Mode 1 where the falling edge of $\overline{\text{CONVST}}$ starts conversion and puts the Track/Hold amplifier into its hold mode. This falling edge of $\overline{\text{CONVST}}$ also causes the BUSY signal to go high to indicate that a conversion is taking place. The BUSY signal goes low when the conversion is complete, which is 5 µs max after the falling edge of $\overline{\text{CONVST}}$ and new data from this conversion is available in the output register of the AD7894. A read operation accesses this data. This read operation consists of 16 clock cycles and the length of this read operation will depend on the serial clock frequency. For the fastest throughput rate (with a serial clock of 16 MHz) the read operation will take 1.0 µs. The read operation must be complete at least 250 ns before the falling edge of the next $\overline{\text{CONVST}}$ and this gives a total time of 6.25 µs for the full throughput time (equivalent to 160 kHz). This mode of operation should be used for high sampling applications.

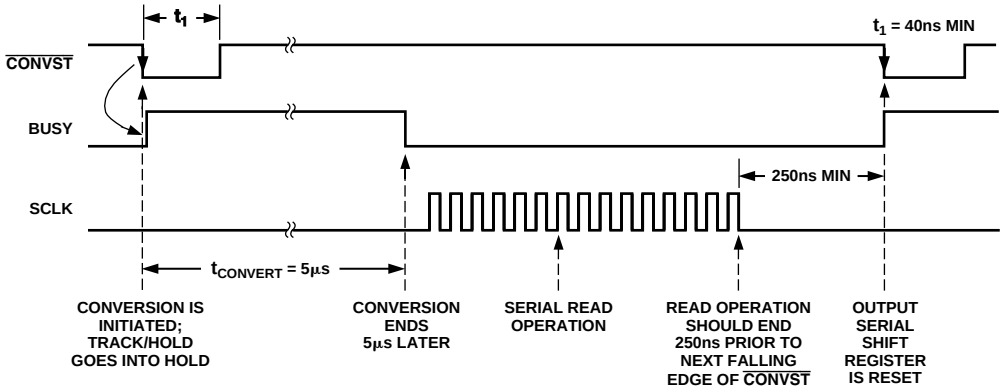


Figure 3. Mode 1 Timing Operation Diagram for High Sampling Performance

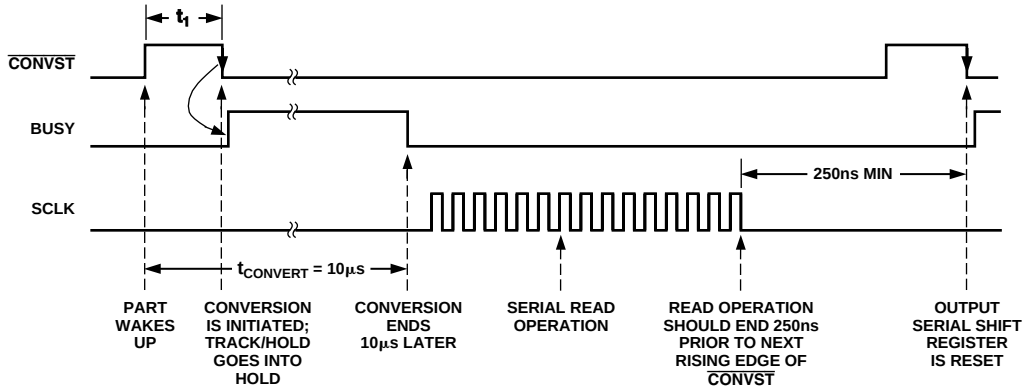


Figure 4. Mode 2 Timing Diagram Where Automatic Sleep Function is Initiated

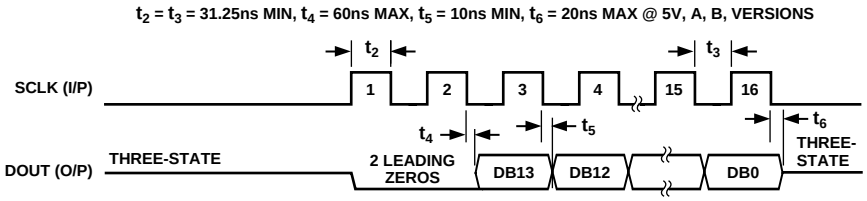


Figure 5. Data Read Operation

Mode 2 Operation (Auto Sleep After Conversion)

The timing diagram in Figure 4 is for optimum performance in operating Mode 2, where the part automatically goes into sleep mode once BUSY goes low, after conversion and "wakes up" before the next conversion takes place. This is achieved by keeping $\overline{\text{CONVST}}$ low at the end of conversion, whereas it was high at the end of conversion for Mode 1 Operation. The rising edge of $\overline{\text{CONVST}}$ "wakes up" the AD7894. This wake-up time is typically 5 µs and is controlled internally by a monostable circuit. While the AD7894 is waking up there is some digital activity internal to the part. If the falling edge of $\overline{\text{CONVST}}$ (putting the track/hold amplifier into hold mode) should occur during this digital activity, noise will be injected into the track/hold amplifier resulting in a poor conversion. For optimum results the $\overline{\text{CONVST}}$ pulse should be between 40 ns and 2 µs or greater than 6 µs in width. The narrower pulse will allow a system to instruct the AD7894 to begin waking up and perform a conversion when ready, whereas the pulse greater than 6 µs will give control over when the sampling instant takes place. Note that the 10 µs wake-up time shown in Figure 4 is for a $\overline{\text{CONVST}}$ pulse less than 2 µs. If a $\overline{\text{CONVST}}$ pulse greater than 6 µs is used, the conversion will not complete for a further 5 µs after the falling edge of $\overline{\text{CONVST}}$. Even though the part is in sleep mode, data can still be read from it. The read operation consists of 16 clock cycles as in Mode 1 Operation. For the fastest serial clock of 16 MHz, the read operation will take 1.0 µs and this must be complete at least 250 ns before the falling edge of the next $\overline{\text{CONVST}}$, to allow the track/hold amplifier to have enough time to settle. This mode is very useful when the part is converting at a slow rate, as the power consumption will be significantly reduced from that of Mode 1 Operation.

Serial Interface

The serial interface to the AD7894 consists of just three wires, a serial clock input (SCLK) and the serial data output (SDATA) and a conversion status output (BUSY). This allows for an easy-to-use interface to most microcontrollers, DSP processors and shift registers.

Figure 5 shows the timing diagram for the read operation to the AD7894. The serial clock input (SCLK) provides the clock source for the serial interface. Serial data is clocked out from the SDATA line on the falling edge of this clock and is valid on both the rising and falling edges of SCLK. The advantage of having the data valid on both the rising and falling edges of the SCLK is to give the user greater flexibility in interfacing to the part and so a wider range of microprocessor and microcontroller interfaces can be accommodated. This also explains the two timing figures, t_4 and t_5, that are quoted on the diagram. The time t_4 specifies how long after the falling edge of the SCLK the next data bit becomes valid, whereas the time t_5 specifies for how long after the falling edge of the SCLK the current data bit is valid. The first leading zero is clocked out on the first rising edge of SCLK. Note that the first zero will be valid on the first falling edge of SCLK even though the data access time is specified at 60 ns for the other bits. The reason for this is that the first bit will be clocked out faster than the other bits is due to the internal architecture of the part. Sixteen clock pulses must be provided to the part to access to full conversion result. The AD7894 provides two leading zeros followed by the 14-bit conversion result starting with the MSB (DB13). The last data bit to be clocked out on the penultimate falling clock edge is the LSB (DB0). On the 16th falling edge of SCLK the LSB (DB0) will be valid for a specified time to allow the bit to be read on the falling edge of the SCLK and then the SDATA line is disabled (three-stated). After this last bit has been clocked out, the SCLK input should return low and remain low until the next serial data read operation. If there are extra clock pulses after the 16th clock, the AD7894 will start over again with outputting data from its output register and the data bus will no longer be three-stated even when the clock stops. Provided the serial clock has stopped before the next falling edge of

$\overline{\text{CONVST}}$, the AD7894 will continue to operate correctly with the output shift register being reset on the falling edge of $\overline{\text{CONVST}}$. However, the SCLK line must be low when $\overline{\text{CONVST}}$ goes low in order to reset the output shift register correctly.

The serial clock input does not have to be continuous during the serial read operation. The 16 bits of data (two leading zeros and 14-bit conversion result) can be read from the AD7894 in a number of bytes.

The AD7894 counts the serial clock edges to know which bit from the output register should be placed on the SDATA output. To ensure that the part does not lose synchronization, the serial clock counter is reset on the falling edge of the $\overline{\text{CONVST}}$ input provided the SCLK line is low. The user should ensure that the SCLK line remains low until the end of the conversion. When the conversion is complete, BUSY goes low, the output register will be loaded with the new conversion result and can be read from with 16 clock cycles of SCLK.

MICROPROCESSOR/MICROCONTROLLER INTERFACE

The AD7894 provides a two-wire serial interface that can be used for connection to the serial ports of DSP processors and microcontrollers. Figures 6 through 9 show the AD7894 interfaced to a number of different microcontrollers and DSP processors. The AD7894 accepts an external serial clock and as a result, in all interfaces shown here, the processor/controller is configured as the master, providing the serial clock, with the AD7894 being the slave in the system. The BUSY signal need not be used for a two-wire interface if the read can be timed to occur 5 μs after the start of conversion (assuming Mode 1 operation).

AD7894 to 8X51/L51 Interface

Figure 6 shows an interface between the AD7894 and the 8X51/L51 microcontroller. The 8X51/L51 is configured for its Mode 0 serial interface mode. The diagram shows the simplest form of the interface where the AD7894 is the only part connected to the serial port of the 8X51/L51 and, therefore, no decoding of the serial read operations is required.

To select the AD7894 in systems where more than one device is connected to the 8X51/L51's serial port, a port bit, configured as an output from one of the 8X51/L51's parallel ports, can be used to gate on or off the serial clock to the AD7894. A simple AND function on this port bit and the serial clock from the 8X51/L51 will provide this function. The port bit should be high to select the AD7894 and low when it is not selected.

The end of conversion can be monitored by using the BUSY signal, which is shown in the interface diagram of Figure 6. With the BUSY line from the AD7894 connected to the Port P1.2 of the 8X51/L51 the BUSY line can be polled by the 8X51/L51. The BUSY line can be connected to the $\overline{\text{INT1}}$ line of the 8X51/L51 if an interrupt driven system is preferred. These two options are shown on the diagram.

Note also that the AD7894 outputs the MSB first during a read operation while the 8X51/L51 expects the LSB first. Therefore, the data that is read into the serial buffer needs to be rearranged before the correct data format from the AD7894 appears in the accumulator.

The serial clock rate from the 8X51/L51 is limited to significantly less than the allowable input serial clock frequency with which the AD7894 can operate. As a result, the time to read data from the part will actually be longer than the conversion time of the part. This means that the AD7894 cannot run at its maximum throughput rate when used with the 8X51/L51.

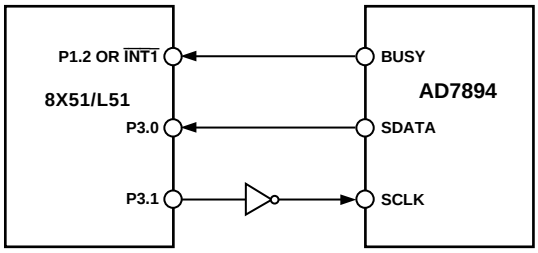


Figure 6. AD7894 to 8X51/L51 Interface

AD7894 to 68HC11/L11 Interface

An interface circuit between the AD7894 and the 68HC11/L11 microcontroller is shown in Figure 7. For the interface shown, the 68L11 SPI port is used and the 68L11 is configured in its single-chip mode. The 68L11 is configured in the master mode with its CPOL bit set to a logic zero and its CPHA bit set to a logic one. As with the previous interface, the diagram shows the simplest form of the interface where the AD7894 is the only part connected to the serial port of the 68L11 and therefore no decoding of the serial read operations is required.

Once again, to select the AD7894 in systems where more than one device is connected to the 68HC11's serial port, a port bit, configured as an output from one of the 68HC11's parallel ports, can be used to gate on or off the serial clock to the AD7894. A simple AND function on this port bit and the serial clock from the 68L11 will provide this function. The port bit should be high to select the AD7894 and low when it is not selected.

The end of conversion is monitored by using the BUSY signal, which is shown in the interface diagram of Figure 7. With the BUSY line from the AD7894 connected to the Port PC2 of the 68HC11/L11 the BUSY line can be polled by the 68HC11/L11. The BUSY line can be connected to the $\overline{\text{IRQ}}$ line of the 68HC11/L11 if an interrupt driven system is preferred. These two options are shown in the diagram.

The serial clock rate from the 68HC11/L11 is limited to significantly less than the allowable input serial clock frequency with which the AD7894 can operate. As a result, the time to read data from the part will be longer than the conversion time of the part. This means that the AD7894 cannot run at its maximum throughput rate when used with the 68HC11/L11.

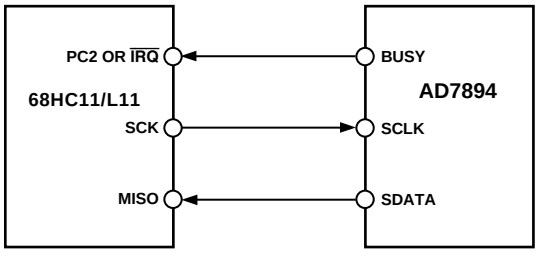


Figure 7. AD7894 to 68HC11/L11 Interface

AD7894 to ADSP-2101/5 Interface

An interface circuit between the AD7894 and the ADSP-2101/5 DSP processor is shown in Figure 8. In the interface shown, the RFS1 output from the ADSP-2101/5s SPORT1 serial port is used to gate the serial clock (SCLK1) of the ADSP-2101/5 before it is applied to the SCLK input of the AD7894. The RFS1 output is configured for active high operation. The BUSY line from the AD7894 is connected to the $\overline{IRQ2}$ line of the ADSP-2101/5 so that at the end of conversion an interrupt is generated telling the ADSP-2101/5 to initiate a read operation. The interface ensures a noncontinuous clock for the AD7894's serial clock input, with only 16 serial clock pulses provided and the serial clock line of the AD7894 remaining low between data transfers. The SDATA line from the AD7894 is connected to the DR1 line of the ADSP-2101/5's serial port.

The timing relationship between the SCLK1 and RFS1 outputs of the ADSP-2101/5 are such that the delay between the rising edge of the SCLK1 and the rising edge of an active high RFS1 is up to 30 ns. There is also a requirement that data must be set up 10 ns prior to the falling edge of the SCLK1 to be read correctly by the ADSP-2101/5. The data access time for the AD7894 is 60 ns (A, B versions) from the rising edge of its SCLK input. Assuming a 10 ns propagation delay through the external AND gate, the high time of the SCLK1 output of the ADSP-2105 must be ≥ (30 + 60 + 10 + 10) ns, i.e., ≥ 110 ns. This means that the serial clock frequency with which the interface of Figure 8 can work is limited to 4.5 MHz.

Another alternative scheme is to configure the ADSP-2101/5 such that it accepts an external noncontinuous serial clock. In this case, an external noncontinuous serial clock is provided that drives the serial clock inputs of both the ADSP-2101/5 and the AD7894. In this scheme, the serial clock frequency is limited to the processor's cycle rate, up to a maximum of 13.8 MHz.

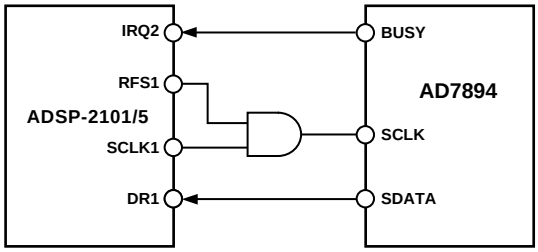


Figure 8. AD7894 to ADSP-2101/5 Interface

AD7894 to DSP56002/L002 Interface

Figure 9 shows an interface circuit between the AD7894 and the DSP56002/L002 DSP processor. The DSP56002/L002 is configured for normal-mode asynchronous operation with gated clock. It is also set up for a 16-bit word with SCK as gated clock output. In this mode, the DSP56002/L002 provides 16 serial clock pulses to the AD7894 in a serial read operation. The DSP56002/L002 assumes valid data on the first falling edge of SCK so the interface is simply three-wire as shown in Figure 9.

The BUSY line from the AD7894 is connected to the MODA/$\overline{IRQA}$ input of the DSP56002/L002 so that an interrupt will be generated at the end of conversion. This ensures that the read operation will take place after conversion is finished.

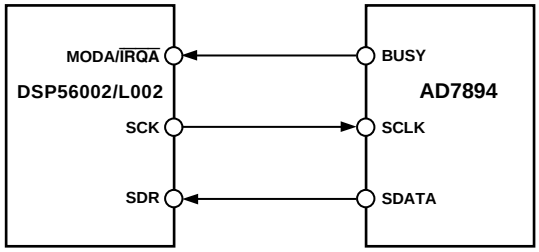


Figure 9. AD7894 to DSP56002/L002 Interface

AD7894 PERFORMANCE

Linearity

The linearity of the AD7894 is determined by the on-chip 14-bit D/A converter. This is a segmented DAC which is laser trimmed for 14-bit integral linearity and differential linearity. Typical relative accuracy numbers for the part are ±1/2 LSB while the typical DNL errors are ±1/3 LSB.

Noise

In an A/D converter, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT, for example) in ac applications. In a sampling A/D converter like the AD7894, all information about the analog input appears in the baseband from dc to 1/2 the sampling frequency. The input bandwidth of the track/hold exceeds the Nyquist bandwidth, so an antialiasing filter should be used to remove unwanted signals above $f_S/2$ in the input signal in applications where such signals exist.

Figure 10 shows a histogram plot for 8192 conversions of a dc input using the AD7894. The analog input was set at the center of a code transition. It can be seen that almost all the codes appear in the one output bin indicating very good noise performance from the ADC.

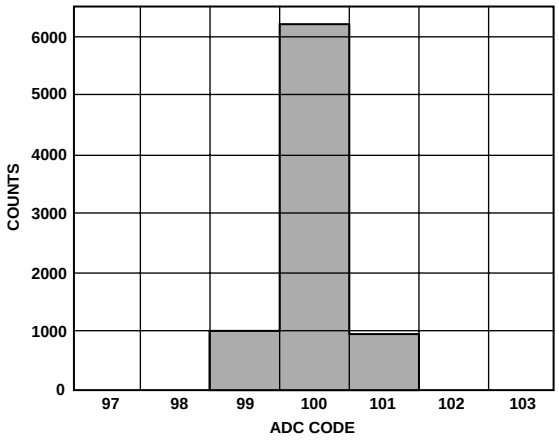


Figure 10. Histogram of 8192 Conversions of a DC Input

Dynamic Performance (Mode 1 Only)

With a conversion time of 5 μs, the AD7894 is ideal for wide bandwidth signal processing applications. These applications require information on the ADC's effect on the spectral content of the input signal. Signal to (Noise + Distortion), Total Harmonic Distortion, Peak Harmonic or Spurious Noise and Intermodulation Distortion are all specified. Figure 11 shows a typical FFT plot of a 10 kHz, ±10 V input after being digitized by the AD7894-10 operating at a 160 kHz sampling rate. The signal to (noise + distortion) ratio is 80.24 dB and the total harmonic distortion is –96.35 dB.

The formula for signal to (noise + distortion) ratio (see Terminology section) is related to the resolution or number of bits in the converter. Rewriting the formula, below, gives a measure of performance expressed in effective number of bits (N):

$$N = \frac{(SNR - 1.76)}{6.02}$$

where *SNR* is Signal to (Noise + Distortion) Ratio.

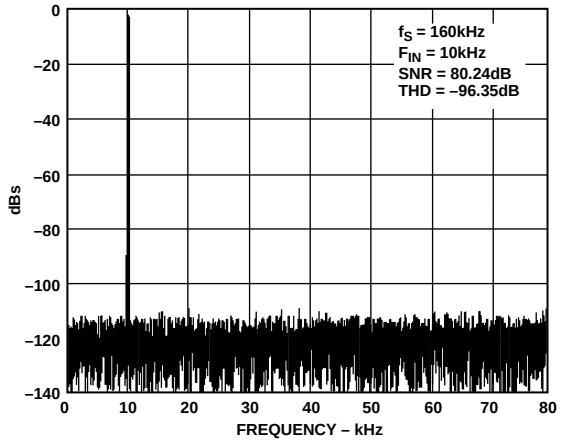


Figure 11. AD7894 FFT Plot

The effective number of bits for a device can be calculated from its measured signal to (noise + distortion) ratio. Figure 12 shows a typical plot of effective number of bits versus frequency for the AD7894 from dc to $f_{SAMPLING}/2$. The sampling frequency is 160 kHz. The plot shows that the AD7894 converts an input sine wave of 10 kHz to an effective numbers of bits of 13.00, which equates to a signal to (noise + distortion) level of 80.02 dB.

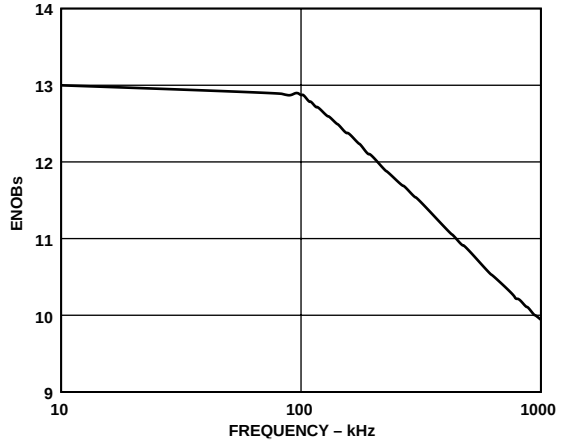


Figure 12. Effective Number of Bits vs. Frequency

Power Considerations

In the automatic power-down mode the part may be operated at a sample rate that is considerably less than 160 kHz. In this case, the power consumption will be reduced and will depend on the sample rate. Figure 13 shows a graph of the power consumption versus sampling rates from 1 Hz to 100 kHz in the automatic power-down mode. The conditions are 5 V supply +25°C. The SCLK pin was held low and no data was read from the part.

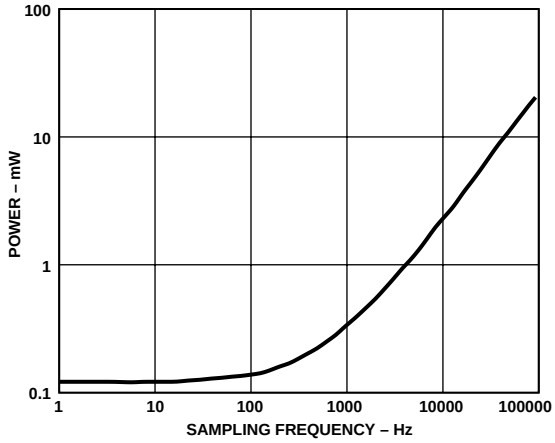


Figure 13. Power vs. Sampling Rate in Automatic Power-Down Mode

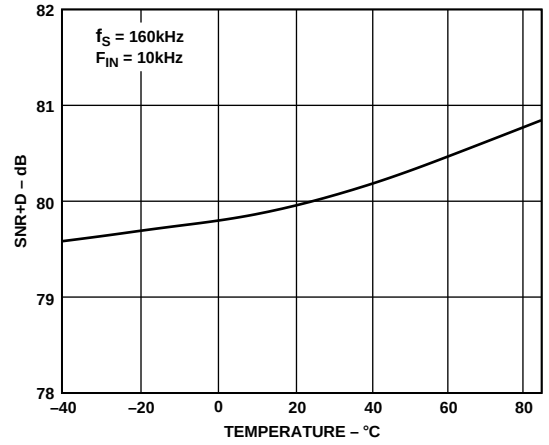


Figure 14. SNR + D vs. Temperature

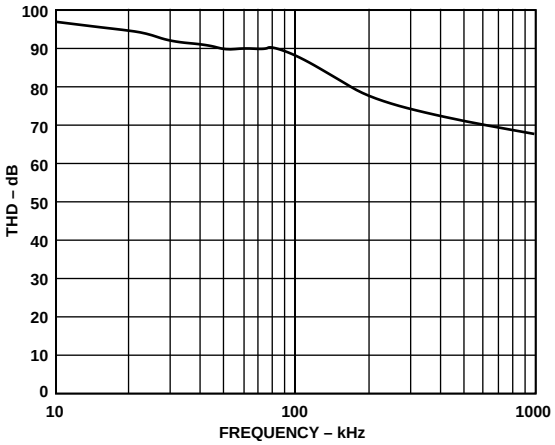
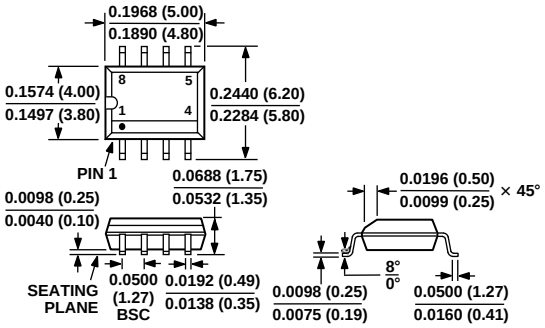


Figure 15. THD vs. Frequency

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Narrow Body SOIC
(SO-8)



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